

IN THE CLAIMS:

Please amend the claims as shown in the following claims listing.

1. (Currently amended) A system, comprising:

a node including an active device, an interface to an inter-node network, a memory, and an address network coupling the active device, the interface, and the memory;

an additional node coupled to the node by the inter-node network;

wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated with the coherency unit, wherein the memory response information includes information used to derive global access state information for the coherency unit;

wherein if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send the additional node a coherency message requesting the access right via the inter-node network.

2. (Original) The system of claim 1, wherein the node includes a data network coupling the active device, the interface, and the memory, and wherein the memory is configured to send the report to the interface in a data packet.

3. (Original) The system of claim 1, wherein the memory response information is configured to identify one of at least two possible response states.

4. (Original) The system of claim 1, wherein if the memory response information indicates a no response state, the memory is configured to send neither the data nor the report in response to the address packet;

wherein when the memory response information indicates the no response state, an additional active device included in the node has an ownership responsibility for the coherency unit and is configured to supply the data to the active device in response to receiving the address packet.

5. (Original) The system of claim 4, wherein if the address packet is conveyed in point-to-point mode by the address network, the memory is configured to send an additional address packet indicating the transaction to the additional active device having the ownership responsibility for the coherency unit.

6. (Original) The system of claim 4, wherein the memory is configured to update the memory response information to indicate the no response state in response to receiving the address packet, and wherein the active device is configured to gain an ownership responsibility for the address packet in response to receiving the address packet.

7. (Original) The system of claim 1, wherein the memory is configured to update the memory response information to indicate a response state in response to receiving an address packet providing the memory with an ownership responsibility for the coherency unit;

wherein if the memory response information identifies the response state, the memory is configured to send the data corresponding to the coherency unit to the active device in response to the address packet.

8. (Original) The system of claim 1, wherein if the memory response information indicates a shared response state, the memory is configured to not send the report and to send the data corresponding to the coherency unit if the access right is a read access right;

wherein if the memory response information indicates the shared response state and the access right is a write access right, the memory is configured to not send the data to the active device and to send the report to the interface.

9. (Original) The system of claim 8, wherein the memory is configured to update the response information to indicate the shared response state in response to a proxy address packet sent by the interface indicating that an additional active device in the additional node is requesting read access to the coherency unit.

10. The system of claim 1, wherein if the memory response information indicates an invalid response state, the memory is configured to not send the data to the active device and to send the report to the interface in response to the address packet.

11. (Original) The system of claim 10, wherein the memory is configured to update the memory response information to indicate the invalid response state in response to receiving a proxy address packet from the interface indicating that an additional active device included in the additional node is requesting write access to the coherency unit.

12. (Original) The system of claim 1, wherein the memory is configured to send the data dependent on both the memory response information and a global access state of the coherency unit within the node, wherein the memory is configured to send the report dependent on the global access state.

13. (Original) The system of claim 1, wherein the memory is configured to include a value of the memory response information in the report, wherein the value is a value of

the memory response information before the memory response information is modified in response to the address packet.

14. (Original) The system of claim 13, wherein the interface is configured to maintain a plurality of records in an outstanding transaction queue, wherein each of the plurality of records corresponds to a respective report received from the memory, and wherein the interface is configured to determine a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue.

15. (Original) The system of claim 14, wherein in response to receiving an additional coherency message specifying the coherency unit from the additional node, the interface is configured to select a type of proxy address packet to send on the address network dependent on the global access state.

16. (Currently amended) The system of claim ~~[[13]]~~ 7, wherein if the memory subsequently updates the memory response information again in response to another address packet, the memory is configured to provide a new value of the memory response information to the interface.

17. (Currently amended) A node for use in a multi-node system, the node comprising:

a plurality of devices including a memory, an active device, and an interface to an inter-node network coupling nodes in the multi-node computer system;

an address network configured to convey packets between the plurality of devices;

wherein in response to receiving from the active device an address packet initiating a transaction to gain an access right to a coherency unit, the memory is configured to send data corresponding to the coherency unit to the active device dependent on memory response information associated

with the coherency unit, wherein the memory response information includes information used to derive global access state information for the coherency unit;

wherein if the transaction cannot be satisfied within the node, the memory is configured to forward a report corresponding to the address packet to the interface, wherein in response to the report, the interface is configured to send a coherency message requesting the access right to another one of the nodes via the inter-node network.

18. (Original) The node of claim 17, further comprising a data network coupling the active device, the interface, and the memory, wherein the memory is configured to send the report to the interface in a data packet.

19. (Original) The node of claim 17, wherein the memory response information is configured to identify one of at least two possible response states.

20. (Original) The node of claim 17, wherein if the memory response information indicates a no response state, the memory is configured to send neither the data nor the report in response to the address packet;

wherein when the memory response information indicates the no response state, an additional active device included in the node has an ownership responsibility for the coherency unit and is configured to supply the data to the active device in response to receiving the address packet.

21. (Original) The node of claim 20, wherein if the address packet is conveyed in point-to-point mode by the address network, the memory is configured to send an additional address packet indicating the transaction to the additional active device having the ownership responsibility for the coherency unit.

22. (Original) The node of claim 20, wherein the memory is configured to update the memory response information to indicate the no response state in response to receiving the address packet, and wherein the active device is configured to gain an ownership responsibility for the address packet in response to receiving the address packet.

23. (Original) The node of claim 17, wherein the memory is configured to update the memory response information to indicate a response state in response to receiving an address packet providing the memory with an ownership responsibility for the coherency unit;

wherein if the memory response information identifies the response state, the memory is configured to send the data corresponding to the coherency unit to the active device in response to the address packet.

24. (Original) The node of claim 17, wherein if the memory response information indicates a shared response state, the memory is configured to send the data corresponding to the coherency unit if the access right is a read access right;

wherein if the memory response information indicates the shared response state and the access right is a write access right, the memory is configured to send the report to the interface.

25. (Original) The node of claim 24, wherein the memory is configured to update the response information to indicate the shared response state in response to a proxy address packet sent by the interface indicating that an additional active device in another node is requesting read access to the coherency unit.

26. (Original) The node of claim 17, wherein if the memory response information indicates an invalid response state, the memory is configured to send the report to the interface in response to the address packet.

27. (Original) The node of claim 26, wherein the memory is configured to update the memory response information to indicate the invalid response state in response to receiving a proxy address packet from the interface indicating that an additional active device included in another node is requesting write access to the coherency unit.
28. (Original) The node of claim 17, wherein the memory is configured to send the data dependent on both the memory response information and a global access state of the coherency unit within the node.
29. (Original) The node of claim 17, wherein the memory is configured to include a value of the memory response information in the report, wherein the value is a value of the memory response information before the memory response information is modified in response to the address packet.
30. (Original) The node of claim 29, wherein the interface is configured to maintain a plurality of records in an outstanding transaction queue, wherein each of the plurality of records corresponds to a respective report received from the memory, and wherein the interface is configured to determine a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue.
31. (Original) The node of claim 30, wherein in response to receiving an additional coherency message specifying the coherency unit from another node, the interface is configured to select a type of proxy address packet to send on the address network dependent on the global access state.
32. (Currently amended) The node of claim ~~[[14]]~~ 22, wherein if the memory subsequently updates the memory response information again in response to another address packet, the memory is configured to provide a new value of the memory response information to the interface.

33. (Currently amended) A method of operating a multi-node system, wherein the multi-node system includes a node and an additional node coupled by an inter-node network, the method comprising:

an active device included in the node initiating a transaction to gain an access right to a coherency unit by sending an address packet on an address network included in the node;

dependent on memory response information associated with the coherency unit, a memory included in the node sending data corresponding to the coherency unit to the active device in response to the address packet, wherein the memory response information includes information used to derive global access state information for the coherency unit;

if the transaction cannot be satisfied within the node, the memory forwarding a report corresponding to the address packet to the interface;

in response to the report, the interface sending the additional node a coherency message requesting the access right via the inter-node network.

34. (Original) The method of claim 33, wherein said forwarding the report comprises the memory send a data packet including the report to the interface via a data network included in the node.

35. (Original) The method of claim 33, wherein the memory response information identifies one of at least two possible response states.

36. (Original) The method of claim 33, wherein if the memory response information indicates a no response state, the memory sends neither the data nor the report in response to the address packet;

wherein when the memory response information indicates the no response state, an additional active device included in the node has an ownership responsibility for the coherency unit and supplies the data to the active device in response to receiving the address packet.

37. (Original) The method of claim 36, further comprising: the memory sending an additional address packet indicating the transaction to the additional active device having the ownership responsibility for the coherency unit if the address packet is conveyed in point-to-point mode by the address network.

38. (Original) The method of claim 36, further comprising:

the memory updating the memory response information to indicate the no response state in response to receiving the address packet; and

the active device gaining an ownership responsibility for the address packet in response to receiving the address packet.

39. (Original) The method of claim 33, further comprising:

the memory updating the memory response information to indicate a response state in response to receiving an address packet providing the memory with an ownership responsibility for the coherency unit;

wherein if the memory response information identifies the response state, the memory sends the data corresponding to the coherency unit to the active device in response to the address packet.

40. (Original) The method of claim 33, wherein if the memory response information indicates a shared response state, the memory does not send the report and sends the data corresponding to the coherency unit if the access right is a read access right;

wherein if the memory response information indicates the shared response state and the access right is a write access right, the memory does not send the data to the active device and sends the report to the interface.

41. (Original) The method of claim 40, further comprising the memory updating the response information to indicate the shared response state in response to a proxy address packet sent by the interface indicating that an additional active device in the additional node is requesting read access to the coherency unit.
42. (Original) The method of claim 33, wherein if the memory response information indicates an invalid response state, the memory does not send the data to the active device and sends the report to the interface in response to the address packet.
43. (Original) The method of claim 42, further comprising the memory updating the memory response information to indicate the invalid response state in response to receiving a proxy address packet from the interface indicating that an additional active device included in the additional node is requesting write access to the coherency unit.
44. (Original) The method of claim 33, wherein the memory sends the data dependent on both the memory response information and a global access state of the coherency unit within the node, wherein the memory sends the report dependent on the global access state.
45. (Original) The method of claim 33, further comprising the memory including a value of the memory response information in the report, wherein the value is a value of the memory response information before the memory response information is modified in response to the address packet.
46. (Original) The method of claim 45, further comprising:

the interface maintaining a plurality of records in an outstanding transaction queue, wherein each of the plurality of records corresponds to a respective report received from the memory; and

the interface determining a global access state of the coherency unit in the node from the value of the memory response information included in the report and from one or more of the records in the outstanding transaction queue.

47. (Original) The method of claim 46, further comprising:

in response to receiving an additional coherency message specifying the coherency unit from the additional node, the interface selecting a type of proxy address packet to send on the address network dependent on the global access state.

48. (Currently amended) The method of claim ~~[[46]]~~ 38, further comprising:

if the memory subsequently updates the memory response information again in response to another address packet, the memory providing a new value of the memory response information to the interface.